REMARKS

STATUS OF THE CLAIMS

Claims 1-6, 13-18, 20-22, and 24-28 are pending in the application.

Claims 13-18, 20-22, and 24-28 are allowed.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (6,167,479) in view of Kim (6,343,353).

Dependent claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 1 is cancelled without prejudice or disclaimer, claims 2-6 are amended, and new claim 32 is added, and, thus, claims 2-6, 13-18, 20-22, 24-28 and 32 remain pending for reconsideration, which is respectfully requested.

No new matter has been added.

REJECTION

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (6,167,479) in view of Kim (6,343,353). Dependent claim 6 depending from claim 1 is objected to as being allowable if rewritten into independent form. According to the foregoing, objected to dependent claim 6 is amended into independent form and as further amended to use the infinitive form "to —" vs. the gerund form "—ing" (e.g., a control unit ~~processing~~to process ..."), and thus, it is understood that claim 6 and now dependent claims 2-5 therefrom are in condition for allowance.

New claim 32 provides an alternative recitation of the present invention and is allowable over the relied upon references, because it recites patentably distinguishing features of its own as discussed herein. Support for the new claim 32 can be found, for example, in the paragraph spanning pages 21-22, paragraph spanning pages 22-23 and pages 38, line 12 to page 40, line 23 and FIGS. 9 and 10 (e.g., registers 1071 and/or 1072).

In particular, the Office Action maintains from the previous Office Action rejection of claims 1-5 under 35 USC 103(a) as being unpatentable over Hartnett (US Patent No. 6,167,479)

and Kim (US Patent No. 6,343,353). Page 4, item 6, of the Office Action, is the response to previous amended feature of "when it becomes possible to issue an immediately subsequent instruction that is the same ~~instructions~~ as the instruction of said specific application-purpose instruction operation unit" (previously amended claim 1).

The Office Action newly refers to Hartnett's FIG. 3 by alleging, "Hartnett also taught the issuing of immediate instruction which the same as the specific instruction (see the Instruction cycle of subsequent instruction N+1 In fig. 3)." The Office Action rejection in page 4, item 6, by referring to Hartnett's FIG. 3, the paragraphs spanning columns 6 and 7, is not very clear, and it appears that the rejection rationale essentially relies on Hartnett's FIG. 5 and column 7, lines 56-67. In particular, the Office Action in page 3, item 4, maintains that Hartnett discusses the present invention's prescribing a number of cycles, but that Hartnett does not specifically show a writable register for prescribing the number of cycles and that Hartnett does not show hardware to store the number of cycles. So the Office Action relies on Kim for discussing a writeable register.

However, Hartnett's descriptions in column 6 and 7, which is relied upon by the Office Action, relate to standard instruction pipelining and handling non-standard extended-cycle instructions that require more time to complete (column 6, lines 38-46 and column 7, lines 39-55). In contrast to Hartnett, the claimed present invention provides, "***a rewritable register to prescribe for said specific application-purpose operator,*** which executes an operation of the specific application-purpose operation instruction for each application field***, an instruction latency parameter for a specific application-purpose operator instruction that occupies an operating unit source***" (e.g., new claim 32). In other words, according to the present invention, "***an instruction latency parameter***" is prescribed for ***an instruction of said specific application-purpose instruction operator*** or ("***a rewritable register to prescribe ... an instruction latency parameter for a specific application-purpose operator instruction that occupies an operating unit source***" (e.g., new claim 32)), whereas Hartnett handles non-standard or extended cycle instructions.

It is readily apparent that Hartnett fails to contemplate the claimed present invention's, "***a rewritable register to prescribe for said specific application-purpose instruction operator ... an instruction latency parameter for a specific application-purpose operator instruction that occupies an operating unit source*** " (e.g., new claim 32), because Hartnett

does not discuss handling ***an instruction of said specific application-purpose instruction operator***. Further, Hartnett's processing of interrupts discussed in columns 9-15, differs from the claimed present invention's, "***a rewritable register to prescribe for said specific application-purpose instruction operator ... an instruction latency parameter for a specific application-purpose operator instruction that occuples an operating unit source***" (e.g., new claim 32), because Hartnett relates to handling an interrupt and retuning to a state that existed prior to the interrupt (column 9, lines 34-44 and column 10, lines 34-38).

In particular, Hartnett's discussion regarding the N+1 Instruction all relate to the N+1 Instruction prior to an interrupt and for recovery purposes. For example, Hartnett's column 14, lines 39-51, discusses:

> Assuming that a non-fault interrupt is selected by Encode Logic 230 as the next interrupt to process, Interrupt Control Logic 232 is signaled of the interrupt occurrence. Because the interrupt is a non-fault interrupt, Interrupt Control Logic does not generate the Early Abort Signal on Line 216 until the 3X2B phase of Instruction N execution as illustrated by Line 276. This allows the execution of Instruction N to complete. It will be noted that if Instruction N is an extended-cycle instruction as indicated by ones of the Control Lines 176, Interrupt Control Logic 232 must delay the generation of the Early Abort Signal a predetermined number of additional stages as determined by the number of extended stages included in extended-cycle Instruction N.

However, Hartnett is silent on and fails to disclose or suggest the claimed present invention's setting parameters relating to a latency of instruction issue control of the CPU for an instruction of said specific application-purpose instruction operator. In other words, Hartnett fails to disclose or suggest setting any latency parameters for an instruction executed by an interrupt handler.

Further, it is readily apparent that Hartnett's Interrupt Testing Mechanism discussed in columns 18-24 fails to disclose or suggest the claimed present invention.

It is readily apparent, as discussed in the previous Amendment, that Kim fails to disclose or suggest the claimed present invention. Kim, which is relied upon by the Office Action in page 3 to meet the claimed present invention's "***a rewritable register prescribing a number of cycles***" in claim 6, is directed to a micro-controller access to an external memory according to the characteristics of the external memory (Abstract, column 2, lines 23-53). In particular, Kim discusses an MCU capable of accessing an external memory having a different access time

using a microcode (column 3, lines 11-19) and discusses a WAIT register for cycle extension data (columns 3 and 4). However, Kim's cycle extension relates to accessing external memory, and Kim fails to disclose or suggest and differs from the claimed present invention's, "***a rewritable register to prescribe for said specific application-purpose instruction operator***, which executes an operation of the specific application-purpose operation instruction for each application field, ***an instruction latency parameter for a specific application-purpose operator instruction that occupies an operating unit source*** " (e.g., new claim 32).

The foregoing remarks concerning patentably distinguishing features recited in new independent claim 32 (e.g., "***a rewritable register to prescribe ... an instruction latency parameter for a specific application-purpose operator instruction that occupies an operating unit source***" as recited in the claims) also generally apply to patentably distinguishing features recited in claim 1, as now incorporated into claim 6, and to dependent claims 2-5.

Therefore, in contrast to Hartnett and Kim, the claimed present invention as recited in new independent claim 32 provides:

> 32. (NEW) An apparatus, comprising:
>
> a controller to process an operation instruction, which does not have a functional specification, as a specific application-purpose operation instruction;
>
> a specific application-purpose operator to support a flexible pipeline structure and to execute an operation of the specific application-purpose operation instruction for each application field; and
>
> a rewritable register ***to prescribe for said specific application-purpose operator***, which executes an operation of the specific application-purpose operation instruction for each application field, ***an instruction latency parameter for a specific application-purpose operator instruction that occupies an operating unit source.***

In view of the claim amendments and remarks, withdrawal of the rejection of pending claims and allowance of pending claims, including new claim 32, is respectfully requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Respectfully submitted,
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